CS – 09 : Computer Organization & Architecture

Objective: To understand hardware of computer and working of its peripherals.

Unit : 1

Digital Logic Circuits:

- Block diagram of Digital Computers
- Logic Gates :
  - AND
  - OR
  - INVERTER
  - BUFFER
  - NAND
  - NOR
  - XOR
  - XNOR
  - Above gates with graphic symbol, algebraic function and truth table
- Boolean Algebra:

  Boolean Function, truth table, logic diagram, Boolean expression, Basic identities of Boolean algebra, DeMorgans Theorem, Complement of a function, simplification of Boolean expression using Boolean algebra.
- Map Simplification :

  minterms, adjacent squares, two, three and four variable function simplification, product of sum simplification, NAND and NOR implementation, Don't care conditions, example of map simplification using two, three and four variable, sum of product concept.

Unit : 2

Combinational circuits, Flip flop and Sequential circuits:

- Combinational Circuit:
  - Block diagram of Combinational Circuit
  - analysis and design of combinational circuit like Half Adder and Full Adder
- Flip Flops :
  - Concept of Clock pulse
  - SR Flip-flop
  - D Flip-flop
  - JK Flip-flop
  - T Flip-flop
  - Edge-Triggered
  - Master-slave Flip-flop
  - Excitation table of Flip-flop
- Sequential Circuit:
  - Concept and meaning of Sequential circuit
  - Flip-flop Input equation
  - State table
  - State diagram
  - example of Designing of different sequential circuit

Unit : 3

Digital Components:

- Integrated circuits:
  Concept of IC, SSI, MSI, LSI, VLSI, TTL, ECL, MOS, CMOS
- Decoders:
  Concept of decoder, 2 to 4 line decoder, 3 to 8 line decoder, decoder with enable input, NAND gate decoder, Decoder expansion
- Encoders:
  Concept of encoder, Octal to binary encoder
- Multiplexer:
  Concept of Multiplexer, 2 to 1 line multiplexer, 4 to 1 line multiplexer, quadruple 2 to 1 line multiplexer
- De-multiplexer:
  Concept of De-Multiplexer: 1 to 4 line de-multiplexer
- Register:
  Concept of Register, loading of register, 4-bit register, register with parallel load, shift register, bidirectional shift register with parallel load,
- Counter:
  Concept of Binary counter, 4-bit synchronous binary counter, 4-bit binary counter with parallel load

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Unit: 4

Central Processing Unit:

- Introduction of CPU
- Major components of CPU
- Concept of different Computer register
- Registers for the Basic Computer (DR, AR, AC, IR, PC, TR, INPR, OUTR)
- Register symbol, name, number of bits and function is brief
- General Register Organization
  - Control word
- Stack Organization:
  - Register stack
  - Memory stack
  - Polish Notation
- Reverse Polish Notation

Unit: 5

Input-Output Organization and Memory Organization:

Input-Output Organization:

- IO INTERFACE
  - Concept of I/O interface
  - I/O Bus and Interface modules
- I/O versus Memory Bus, example of I/O interface unit
- DMA